SIM5320x SMT Module Design Guide

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Contents

Version History

Data	Version	Description of change	Author
2010-3-18	1.01	Origin	Libing,WangGuizhou
2011-11-07	1.02	Add update and GPS description	Libing

Introduction

This document describes the important points about RF that should be taken into account in client's application design. As SMT module can be integrated with a wide range of applications, the application notes are described in detail.

SMT module is a new and key product which is provided by SIMCom inc. This type module become very popular soon after it is released for its easy integration, good reliability. But bad RF design will lead to serious RF problems. In order to improve the RF performance, this document is formed to give the customer some design guides in RF design of SMT type module integration. Based on such considerations, at the later section, this document will describe some key issues that should be paid more attention to.

1 Scope of the document

This document is intended for the following versions of the SIMCOM modules

- SIM5320A
- SIM5320E
- SIM5320J
- SIM5320C

NOTE: This document can apply for all SMT Modules. SIM5320 is selected as a demonstration in the under sections.

2 Circuit design

When the customer begins to integrate the SMT type module into their product, the first thing to be considered is the circuit design. In this section, we will focus on the circuit design which is related to the RF performance. This section is divided into two sub-parts, the first is the power supply circuit design; the second is the antenna matching circuit design.

2.1 Power supply circuit design

Because the SMT module is a high power consuming communication system, and the maximum working power will up to 2watt in worst case, so, this will form a large voltage drop at the module's power supply port. To make the SMT module have a stabilized working condition, we

recommended a large tantalum capacitor (100uF or more capacity is recommended) shunted to the module's power supply port. To get better noise decoupling performance, some additional small ceramic capacitors can be added combined with the large capacitor.

If the SMT module is powered by a DC-DC in the customer's design, to avoid the module's RF performance is affected by the switching frequency of the DC-DC, for example, modulation spectrum, switching spectrum, a series large current ferrite bead(with rated current minimum 2A) should be added at the power supply port. The recommended power supply circuit is shown as below:

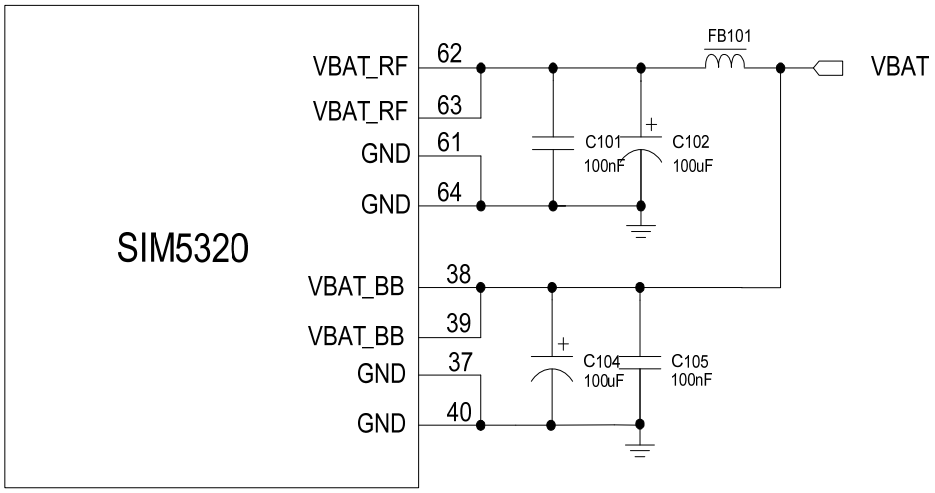


Figure 1: Power supply circuit

In this circuit, by default, the component FB101 should be a 0ohm resistor with 0805 size. When the module is powered by DC-DC, and the module's RF performance is affected by the DC-DC's switching frequency, FB101 can be changed to a large current ferrite bead to filter the noise. We recommend using BLM21PG221SN1 (provided by murata).

2.2 POWER ON/OFF design

The simplest way to turn on/off SIM5320 is driving the POWER_ON to a low level for 64ms then release. POWER_ON pin has been pulled up to 1.8V inside the module. Following figure is the recommended connection with a NPN transistor. User can choose a GPIO of host to control the POWER ON/OFF. Please note that don't add a capacitor on POWER_ON pin, or it may cause some unexpected problems when power on/off process.

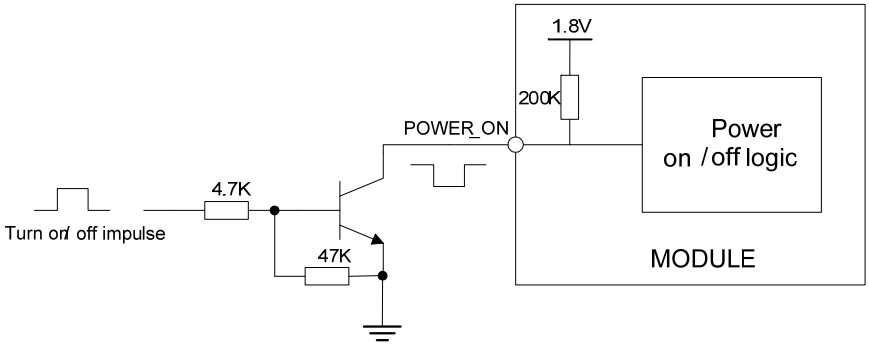


Figure 1: Powered on/down module using transistor

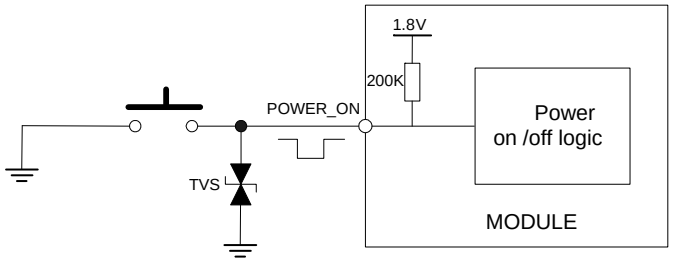


Figure 2: Powered on/down module using button

2.3 Sleep and wake-up design

2.3.1 Sleep mode Design guide

SIM5320x in sleep mode can reduce power consumption. SIM5320x USB interface is connected with a host CPU. SIM5320X could enter sleep mode when the host CPU supports USB suspend mode, otherwise it could not enter sleep mode.
If host CPU don't support USB suspend mode, the SIM5320X module can enter sleep mode by cutting off USB_VBUS line.
NOTE:
1 SIM5320x can not enter sleep mode until module RXD is pulled low.
2 SIM5320x RXD is pulled down by 15k ohm inside SIM5320x. Please don't connect if RXD is not used.
3 Please reference SIM5xxx_sleep_mode_Application_Note for detailed.

2.3.2 Wake up Design guide

SIM5320x can be waked up and drive GPIO41 and RI to low level when it receives a voice or data call and a SMS from network. So user can use SIM5320x GPIO41 or RI pin to wake up host if module and host are both in sleep mode. Host can wake up SIM5320x via pulling our GPIO43 or GPIO0 or DTR low level. Following figures below are the reference circuit and wake-up output behavior.

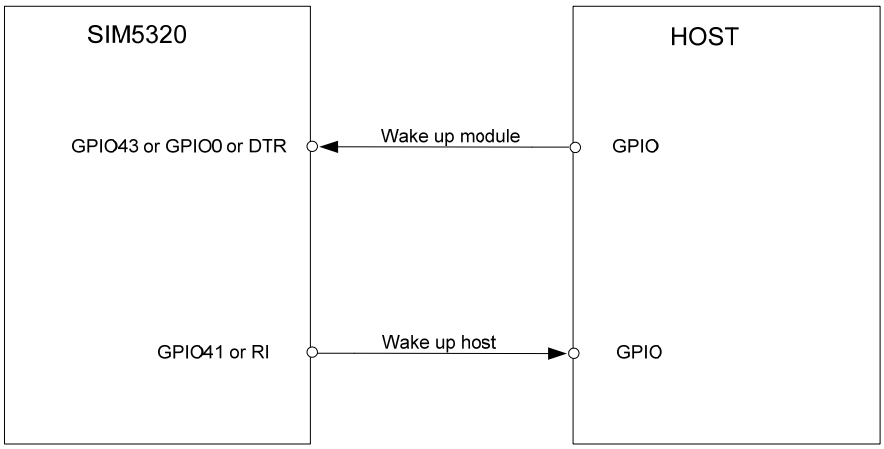


Figure 4: Wake up reference circuit

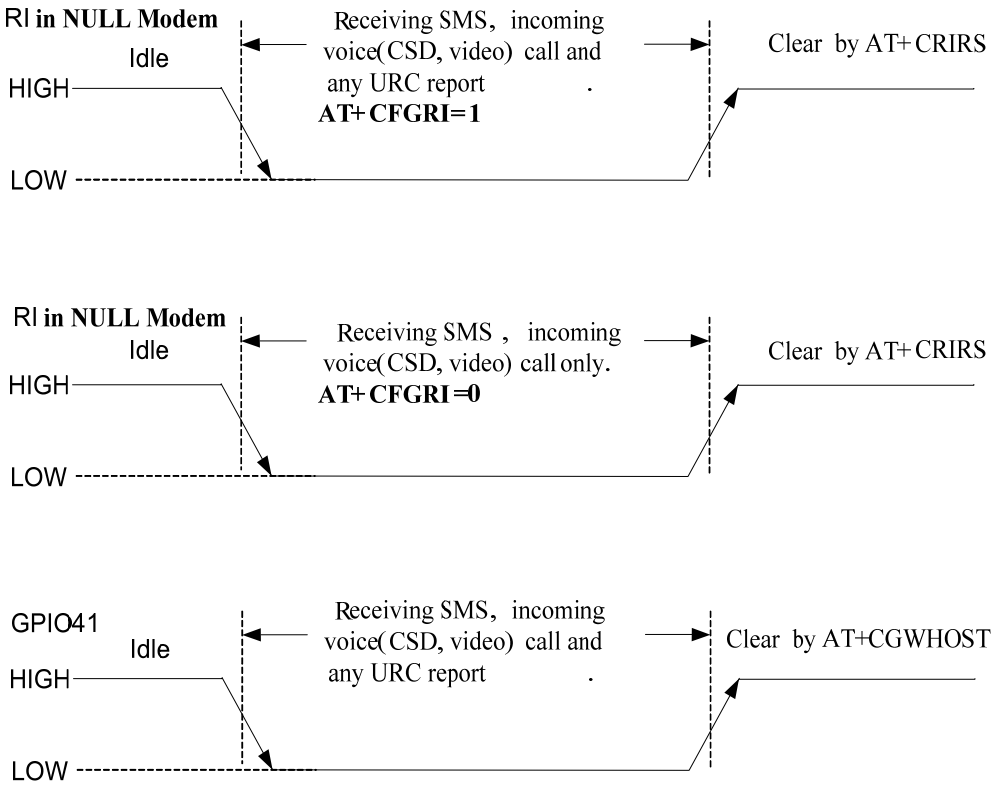


Figure 5: wake-up output behavior.

NOTE: Please reference SIM5320x_Waking_up_Application_Note for detailed.

2.4 SIM card circuit design

The SIM 5320x SIM interface allow the mobile equipment to attach to a GSM or UMTS network.. Both 1.8V and 3.0V SIM card are supported. The SIM interface is powered from an internal regulator in the module.

SIM 5320x does not support SIM detect feature.It's interface has 4 signals:

- V_SIM: SIM power supply.

- USIM_RESET: SIM reset.
- USIM_CLK: SIM clock.
- USIM_DATA: SIM I/O port.

The pull up resistor (15KΩ) on the SIM_DATA line is already added in the module internal. Note that the SIM peripheral circuit should be close to the SIM card socket.
It is recommended to use Transient Voltage Suppressor diodes (TVS)(such as ST ESDA6V1W5 or ON SEMI SMF05C) on the signal connected to the SIM socket in order to prevent any Electrostatics Discharge. TVS diodes with low capacitance (less than 10 pF) have to be connected on USIM_CLK and USIM_DATA signals to avoid any disturbance of the rising and falling edge. These types of diodes are mandatory for the Full Type Approval. They shall be placed as close as possible to the SIM socket.
Some resistors can be added on SIM signals to enhanced EMC and ESD performance. We recommend to use 22 ohm.
The reference circuit of the 8-pin SIM card holder is illustrated in the following figure.

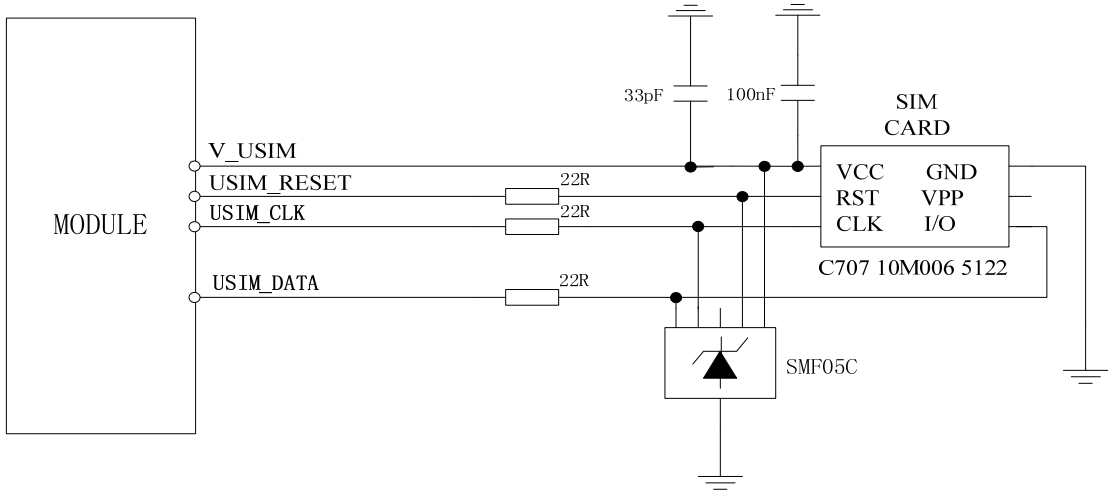


Figure 6: SIM card circuit design

NOTE: If user use an embedded SIM chip, TVS devices is not required. we recommend the 33pf capacitors to add EMC protection and against RF emissions.

2.5 Battery Charge design

SIM5320x do not support the battery charge function. When the Li-ion battery is needed in the application, a charger IC will be implemented. If the battery is only for backup (the AC adaptor is mostly powered), we suggest user choose a charger IC with power-path management for battery lifespan. For example: BQ2407x series from Texas Instruments. Following figure is the reference circuit using BQ24075.

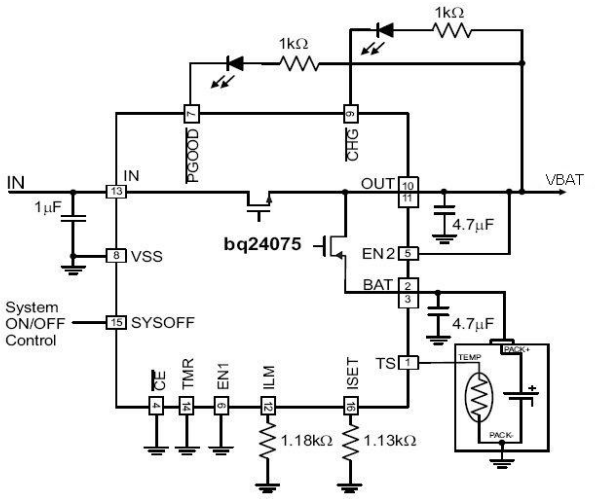


Figure 7: Battery Charge Supply

2.6 Antenna matching circuit design

Because the module is working under 50ohm system in RF part, so, to get the best RF performance, the SMT module's load impedance should be tuned to 50ohm. But in fact, the most antenna's port impedance is not a purely 50ohm, so, to meet the 50ohm requirement, an additional antenna matching circuit should be needed. For the RF test connector, we suggested the customer use the part vended by Murata, its part number is MM8430-2610.The recommended main antenna and GPS antenna matching circuits are shown as below:

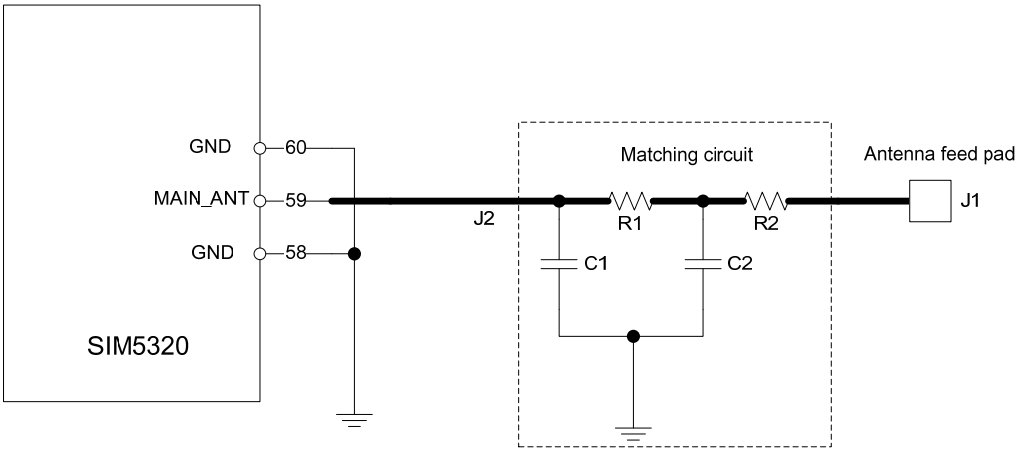


Figure 8: Main antenna matching circuit

In the above Figure, the components R1, C1 and C2 make up a pi-type matching circuit structure. R2 is optional and may be deleted if not used. The RF traces must be 50 ohm impedance controlled in user's PCB design.

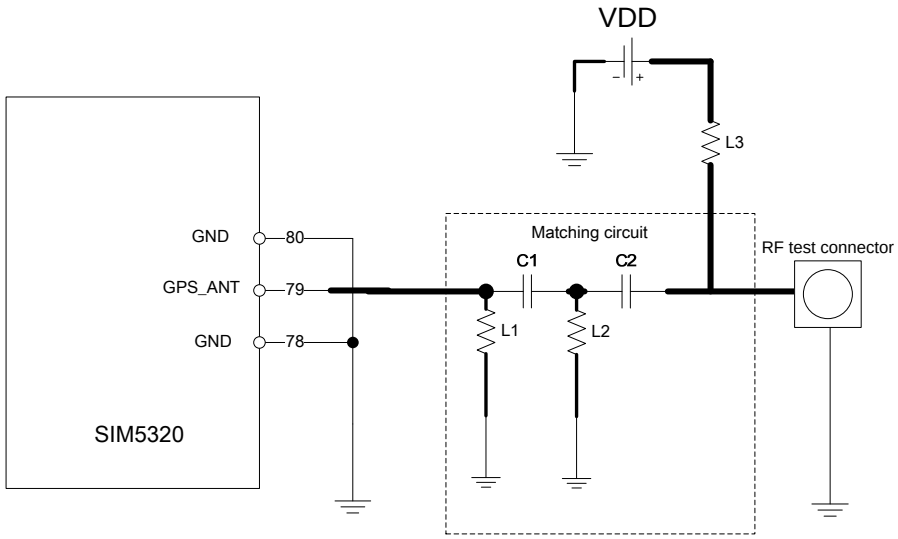


Figure 9: GPS Active antenna circuit

In above Figure, the components C1, and L1, L2 are used for GPS antenna matching, the value of these components depends upon the stack-up layout details and the antenna characteristics. User must pay enough attention to C2 and L3, because the values of these two components depend on the type of antenna. If a passive antenna is used, L3 must be left to NC, C2 can be used as a matching component; but if an active antenna is used, L3 would better be an inductor and C2 must be a capacitor which is used to isolate DC current. It's recommended that L3 using a 47nH inductor and C2 using a 33pf capacitor when active antenna is used.

In active antenna mode, users must provide a VDD which is used to power the active antenna. And this voltage should meet the requirement of active antenna. By the way, VDD should be able to shut down to avoid additional current consumption when GPS is not used.

The RF traces must be 50 ohm impedance controlled in user's PCB design.

If user wants to get better GPS performance, SIMCOM strongly recommended use an external LNA and active antenna, GPS performance will be improved significantly. On the SIM5320 EVB, GPS performance improved by approximately 3db. The recommended GPS circuit is shown as below.

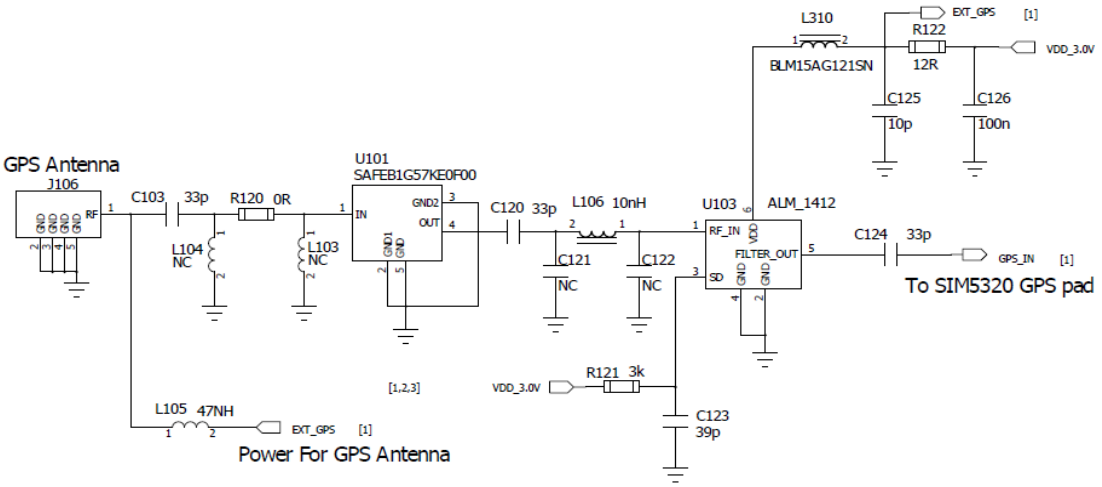


Figure 10: GPS Active antenna circuit（with external LNA）

NOTE: If the GPS antenna is very close to the module, user can choose a passive antenna.

2.7 Firmware update

If SIM 5320x is embed into user's equipment and can't be taken out easily, The module provides two firmware update methods that called USB interface update and FOTA update.

2.7.1 USB interface update

If SIM 5320x communicate with MCU/CPU by hardware UART interface, user can route module USB to a USB-A/USB-B/mini-B slot, and connect USB slot to PC with USB cable. The recommended circuit is shown as below.

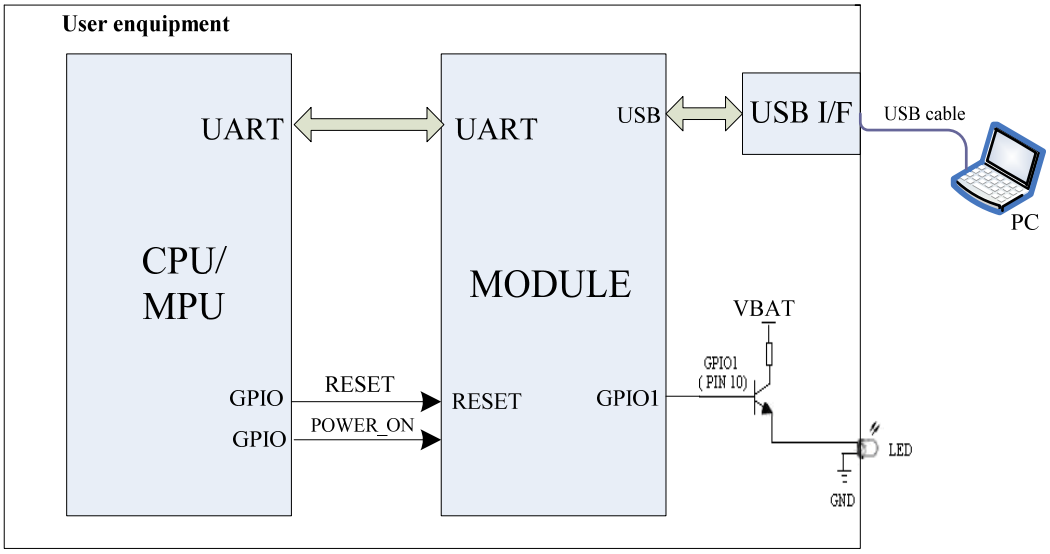


Figure 11：USB interface update reference circuit (UART communicate)

If the host cpu has running wince 、android、linux、win XP or win 7 OS, and communicates with the module using the USB interface. SIMCom provides upgrade tools, which can be compiled into the OS. Upgrade tools can be used to upgrade module with the new firmware.

If SIMCom upgrade tool can not be compiled into host os, user can select a USB 2.0 analog switch if one wants to use USB update. In USB update mode, modules are connected to PC with USB cable by GPIO of CPU/MCU controlling. For USB 2.0 analog switch, User can use ON Semiconductor NLAS7222C. The recommended circuit is shown as below.

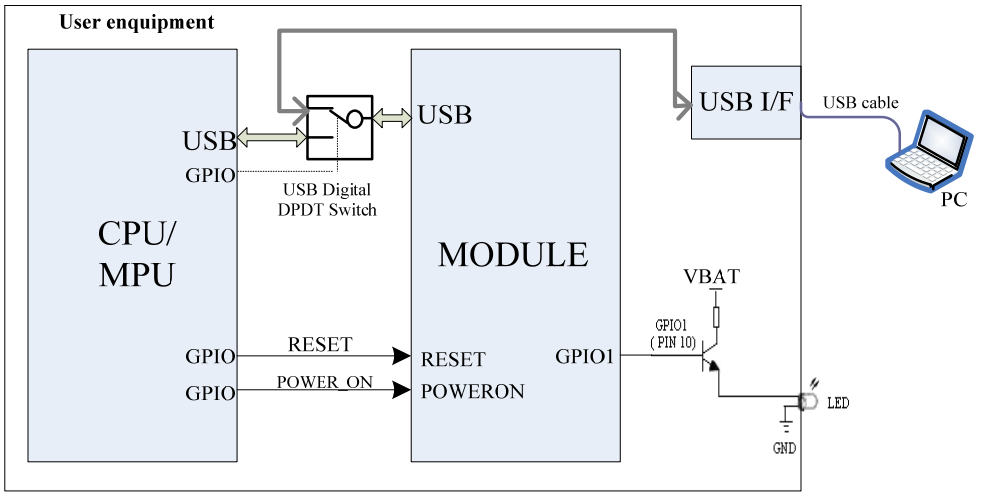
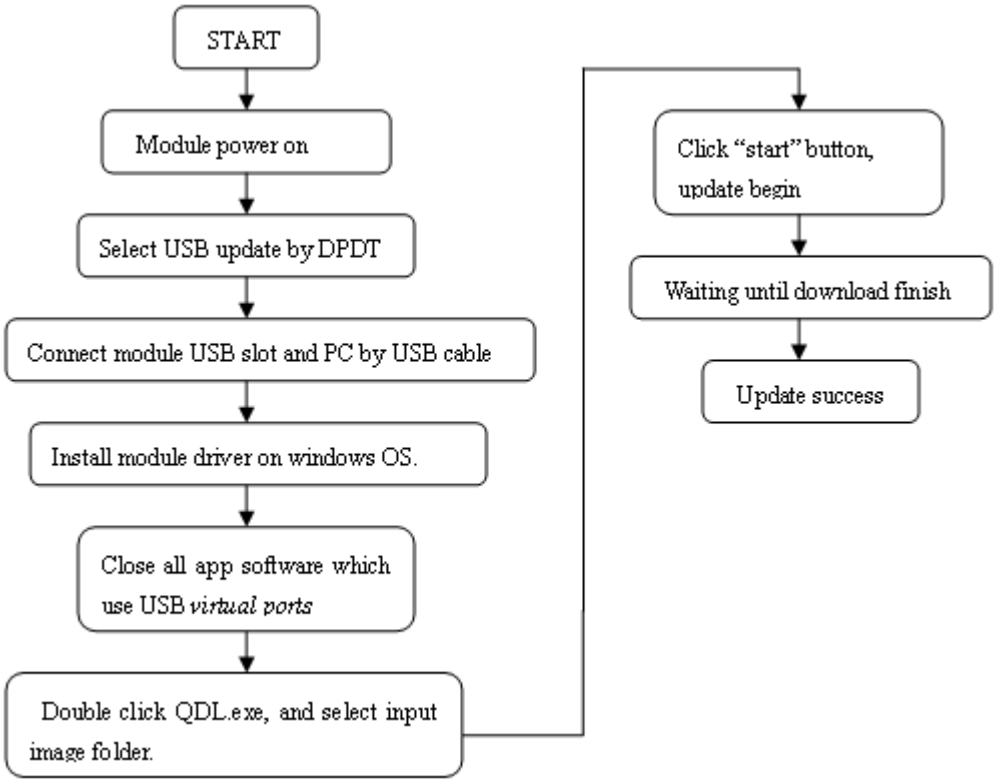


Figure 12：USB interface update reference circuit (USB DPDT switch)



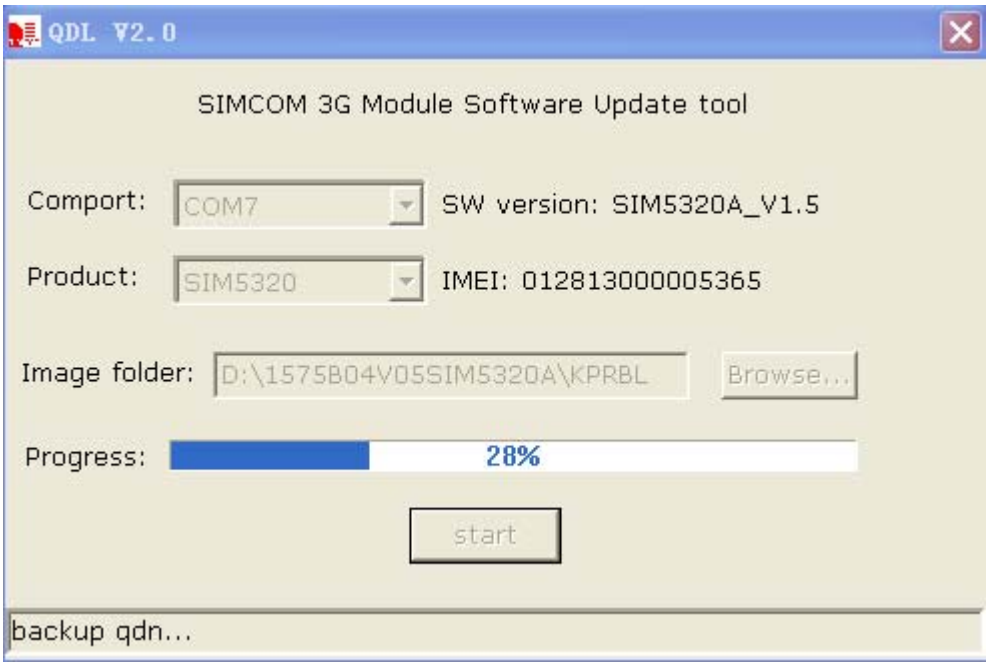


Figure 13：USB interface update procedure

Note: USB 2.0 analog switch chip may add cost.

2.7.2 FOTA update

FOTA update feature can be used to upgrade the module firmware. User wants to know how to use the FOTA update, please contact SIMCom.

Note: network traffic is required when FOTA is used to upgrade the module firmware.

3 Consideration in components and antennas placement

In a PCB design, a good placement of components will help customer to get good performance. The following are some thumbs should be followed.

1）The SMT module should be placed far away from the noise source circuit, such as high speed digital circuit, etc. if this requirement cannot be met, the noise source circuit should be shielded perfectly. This will help to reduce the interference between the SMT module and the noise source circuit.

2）The placement of SMT module should make the module's RF port close to the antenna's feed pad. This will make the length of RF trace between the module's RF port and antenna as short as possible, and consequently.

3）The decoupling capacitor of module's power supply should be placed close to the VBAT pads,

this will help the improvement of decoupling.

4) The antenna must be placed far away from noise source such as: LCD FPC, DCDC circuit, backlight control circuit; antenna also must be far away from the metal components such as: battery, speaker, motor, battery connector, other antennas, LCD and so on.

5) If the GPS function is used, customer's design must account for the transmitter leakage into GPS receiver and if this happens the GPS performance will be drew down. Ideally, the GPS antenna would be placed as far away from the transmitter antennas as possible.

The best placement and some bad placements are shown as below:

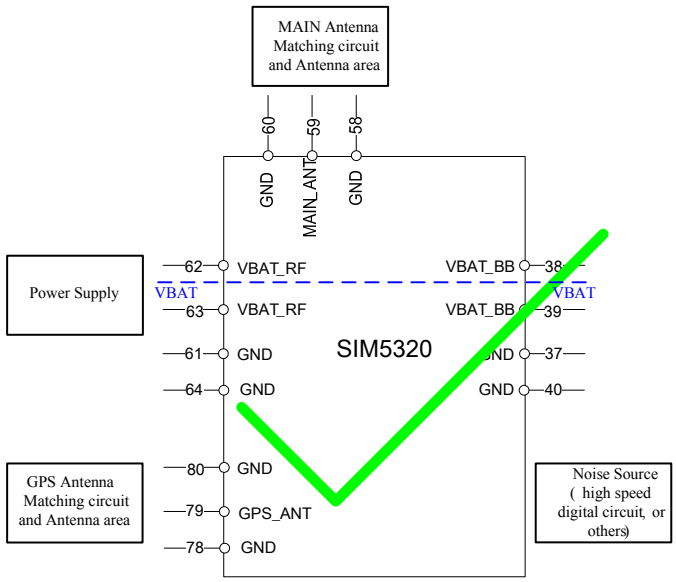


Figure14 Good Placement

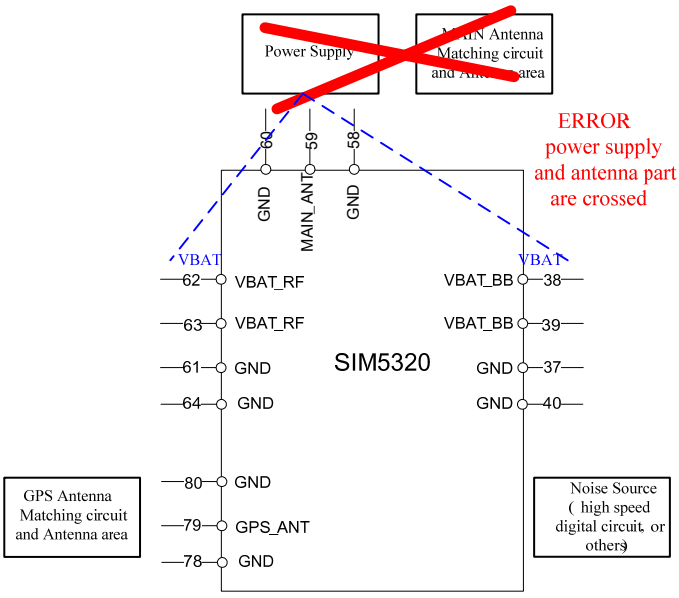


Figure 15 Bad Placement

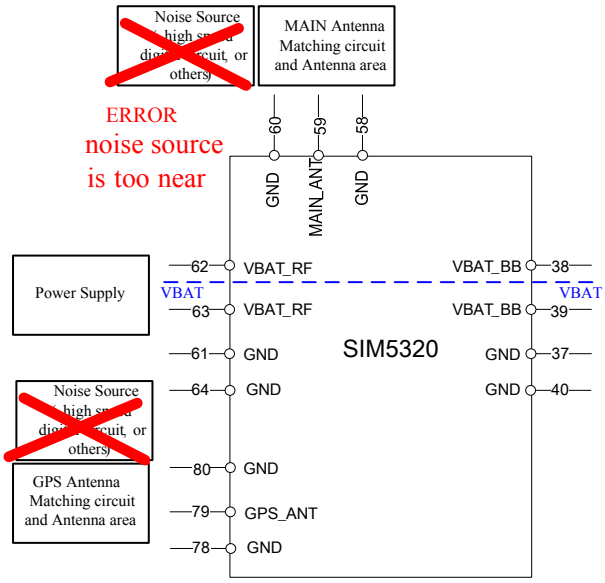


Figure 16 Bad Placement

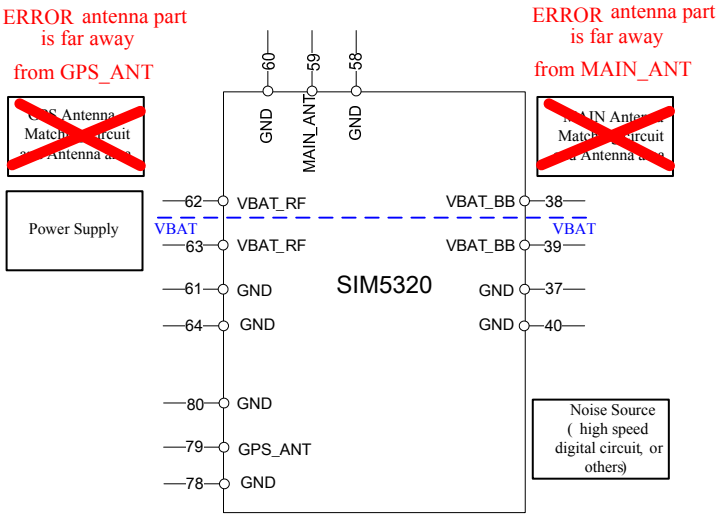


Figure 17 Bad Placement

Figure14 is the best placement; antenna part is near MAIN_ANT pad, power supply is near VBAT pad, noise source is far away the SIM5320.

Figure15, Figure16, Figure17 are bad placements. Figure15, power supply and antenna part are crossed; Figure16, noise source is near to SIM5320; Figure17 antenna part is far away from MAIN_ANT and GPS_ANT pad of SIM5320.

4 Consideration in PCB layout

In product's PCB design, a good PCB layout will help the improvement of the whole product performance, including reliability, EMC performance, etc. The following are some considerations for referenced:

a） The Layer1.under SMT module test port should be copper keep out , layer2 should be GND;

b） The Layer2 under SMT module MAIN_ANT and GPS_ANT pad should be copper keep out , layer3 should be reference GND;

c） The Layer1.Layer2 under RF test connector should be copper keep out, layer3 should be GND; the space to GND plane should more than 0.5mm.

d） RF trace between SMT module RF pad with the RF test connector, RF trace between RF test connector with the antenna matching circuit, RF trace between the antenna matching circuit with the antenna feed PAD all should be controlled to 50 Ohm

e） Avoid to layout any high speed signal under RF trace, if high speed signal is needed, a GND plane is needed between these two signals.

f） All layers under the antenna feed pad should be copper keep out. Or, the space between antenna feed pad with the GND under feed pad should be more than 1mm.

g） Do not layout RF trace in orthogonal.

h） When layout surface Mircostrip Transmission Line or offset Strip Transmission Line , 3W rule should be followed, that means the space between reference GND with RF trace should three times more than the width of RF trace.

i） The VBAT trace should be short and wide, recommended above 80mil.

j） The layout of GROUND is very important. user should keep a full ground on top layer, and most of traces should be layout on the bottom layer, especially the audio traces(MIC & EAR &SPK), keep a whole GROUND under the module shield.

k） The width of MIC& EAR traces should be 8-10mil. The width of SPK traces should be 20 mil. The audio traces had better use difference connection and keep parallel.

l） The ground layer (top , inner layers and bottom) must be connected with many vias.

5 Stacking up of multi-layers PCB

For EMC performance consideration, once the working frequency in the customer's product is over than 5MHz, or the rise-up/fall-down period of digital signal is less than 5ns, then multi-layers PCB should be considered. Now, the more common multi-layer PCB structure is four-layers, six-layers and eight-layers PCB, etc. If the customer's product is designed in multi-layers PCB technology, then the stack-up design of multi-layers PCB will become very important. The following will show some typical stack-up design of multi-layers PCB, but each design has its own advantages and disadvantages.

Note: In the following table, S1 indicates the first signal layer; S2 indicates the second signal layer, and so on.

5.1 Stack-up of two-layers PCB

	Top layer	Bottom layer

Case A	S1+POWER+GND	S2+POWER+GND

Table1 Stack-up of two-layers PCB

Two-layers PCB is the lowest cost solution, but this solution has the worst EMC performance, and it is not appropriate in high speed design, because in this solution, the ground integrity, the crosstalk between signal traces is very bad.

5.2 Stack-up of four-layers PCB

	Top layer	Second layer	Third layer	Bottom layer
Case A	GND	S1+POWER	S2+POWER	GND
Case B	S1	GND	POWER	S2

Table2 Stack-up of four-layers PCB

Case A, should be the best case in four-layers PCB board design. In this case, the outer layer is ground layer, which have some help in shielding the EMI signals; and also, the power supply layer is very close to the ground layer, so the power supply resistance is smaller, and the EMC performance will be very good. But if the density of devices on the PCB is very high, then this type PCB stack-up should not be used to design, because the ground integrity can not be assured under high density design, and the signal quality in second layer will be very bad. In this situation, Case B is the most common way usually.

5.3 Stack-up of six-layers PCB

	Top layer	Second layer	Third layer	Fourth layer	Fifth layer	Bottom layer
Case A	S1	GND	S2	S3	POWER	S4
Case B	S1	S2	GND	POWER	S3	S4
Case C	S1	GND	S2	POWER	GND	S3
Case D	GND	S1	POWER	GND	S2	GND

Table3 Stack-up of six-layers PCB

Six-layers PCB gives more design flexibility than a four-layers PCB, but it takes some work to make it ideal in EMC terms.

Case A in the above table, is the usually common way. In this case, S1 is a better signal routing layer, and S2 somewhat less. But this case has a disadvantage that this stack-up has very little distributed capacitance between its ground and power planes.

Case B has good EMC characteristics, because this stack-up has good noise decoupling between the power plane and ground for the big distributed capacitance.

Case C is the better stack-up, in this case, S1, S2 and S3 are good signal routing layer, the power decoupling is good for the big distributed capacitance between the ground and power planes.

Case D is the best stack-up, the EMC performance will be good, but the disadvantage is that the

routing layer is less than other type stack-up.

5.4 Stack-up of eight-layers PCB

	Top layer	Second layer	Third layer	Forth layer	Fifth layer	Sixth layer	Seventh layer	Bottom layer
A	S1	S2	GND	S3	S4	POWER	S5	S6
B	S1	S2	S3	GND	POWER	S4	S5	S6
C	S1	GND	S2	S3	S4	S5	POWER	S6
D	S1	GND	S2	S3	GND	POWER	S4	S5
E	S1	GND	S2	GND	S3	POWER	S4	S5
F	S1	GND	S2	GND	POWER	S3	GND	S4

Table4 Stack-up of eight-layers PCB

Eight-layers PCB gives more design flexibility than a six-layers PCB, but it takes some work to make it ideal in EMC terms.

If the design needs 6 signal routing layers, then case A will be the best stack-up design, but this type stack-up should not be used in high speed digital circuit design.
If the product design needs 5 signal routing layers, case E will be the best. In this case, S1, S2 and S3 are good signal routing layer, and the power decoupling is good.
If the design needs 4 signal routing layers, case F will be the best. In this case, every signal routing layers are good. In all the case, the signal trace routed in adjacent signal routing layers should be orthogonal.

6 Appendix

6.1 Impedance control of RF trace

Because the module's RF part is working in a 50ohm system, so its output load impedance should be 50ohm, to meet this requirement, the all RF signal trace should be impedance controlled, and its characteristic impedance should be 50ohm.

The RF trace impedance can be controlled through using different trace geometry. There are more than thirty different types of transmission line which can easily be created on a PCB. Twelve of them are shown in figure 18

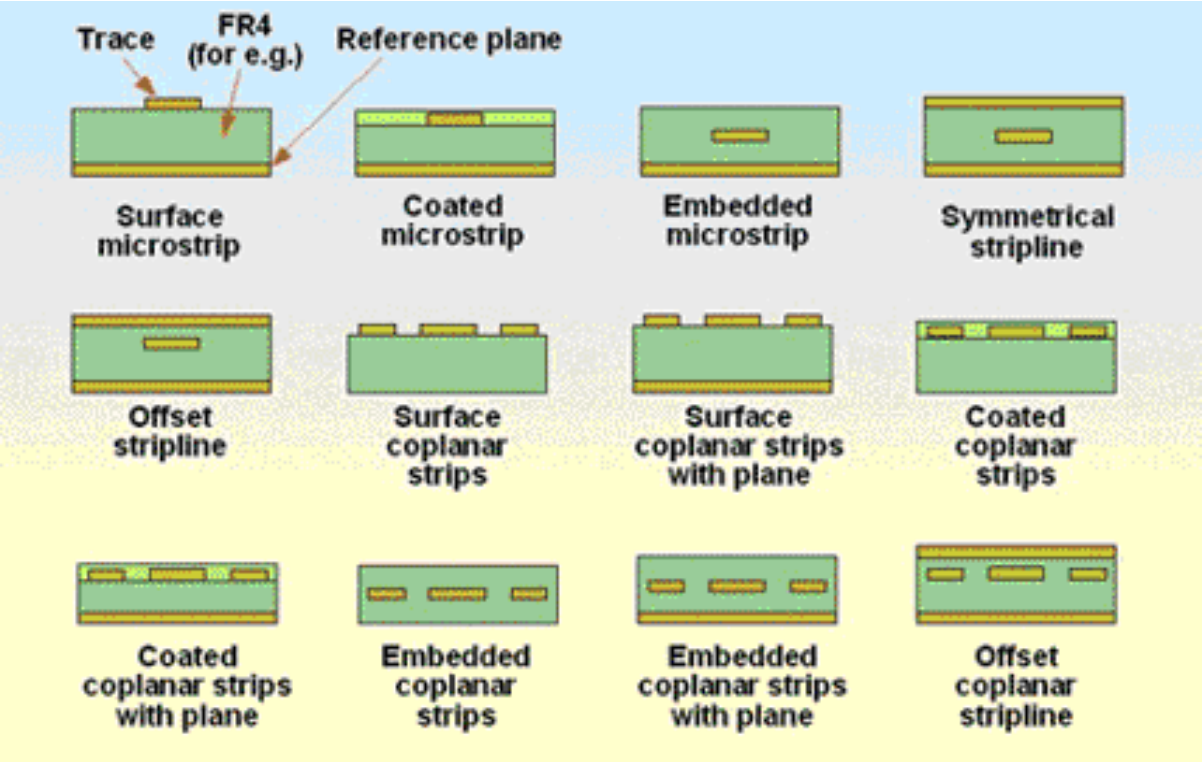


Figure 18: twelve typical PCB transmission line

Usually, Surface Mircostrip Transmission Line and offset Strip Transmission Line are the most common structures. In 50ohm RF system, through adjusting the width of RF traces and the spacing to the reference GND, the impedance of RF traces can be controlled to 50Ohm.The appendix will show some illustration in impedance controlled RF trace designing.

The customer may use software tool to calculate the impedance of RF trace, for example CITS25, released by POLAR, the website is http://www.polarinstruments.com/, or APPCAD released by AGILENT, the website is http://www.hp.woodshot.com.

Here are two examples about using CITS25 to calculate, Surface Mircostrip Transmission Line and Offset strip Transmission Line correspondingly. Based on stack up of six-layers PCB (thickness =1.0mm) shown in appendix.

Surface Mircostrip Transmission Line, the height is 298um (25+70+203=298um), the thickness is 25um, the result width (w) is 584um, as shown in figure 19.

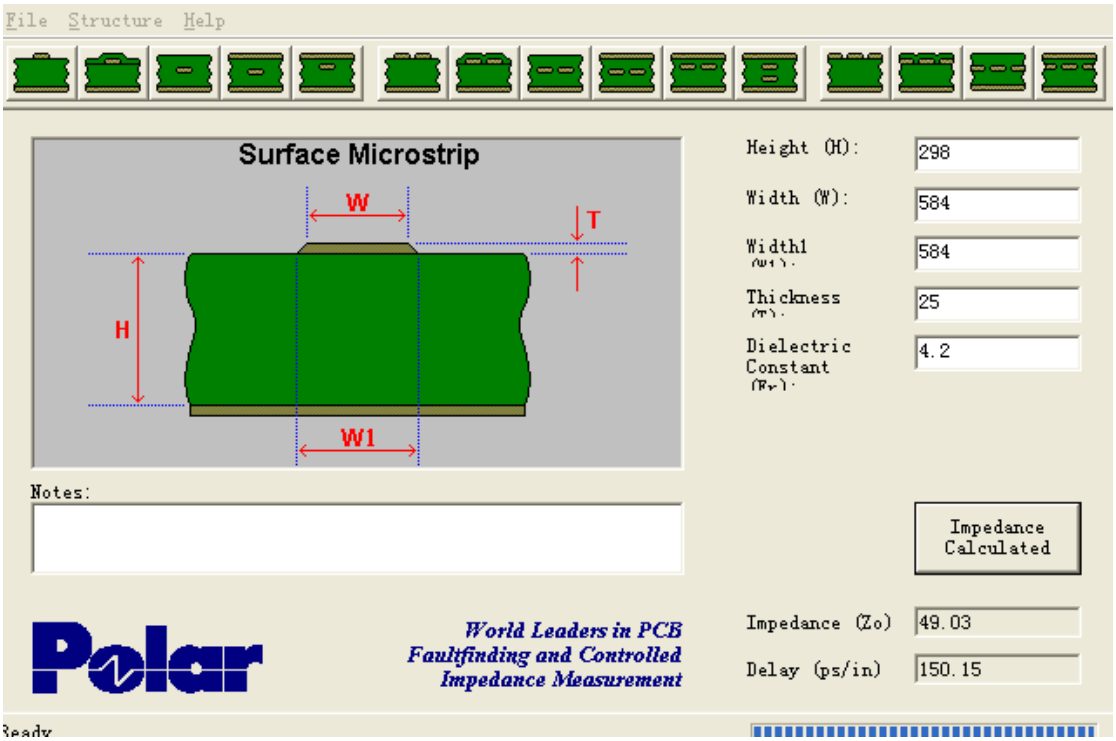


Figure 19: Surface Mircostrip Calculate

Offset Strip Transmission Line，the height between two reference GND is 418um (203+35+180 = 418um), the height between RF trace and reference GND is 180um, the result width is 135um. as shown in figure 20.

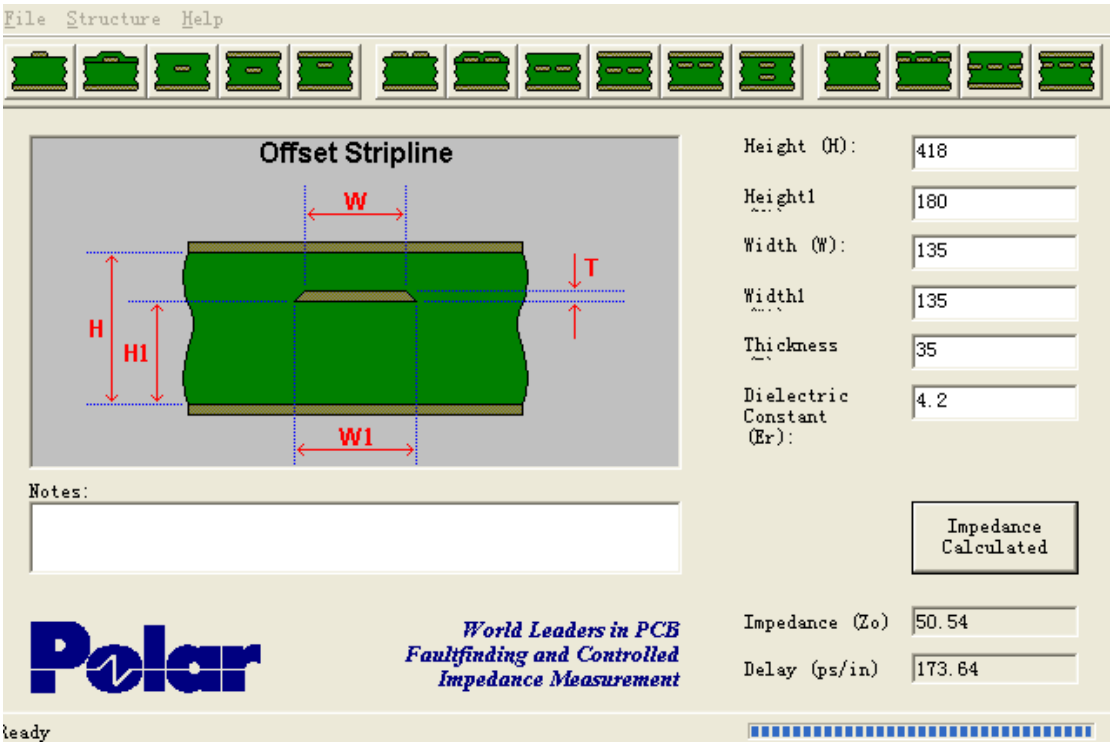


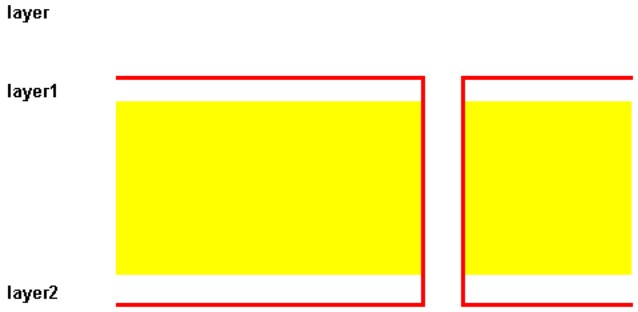
Figure 20: Offset Strip line Calculate

6.2 Example of impedance controlled RF trace

The following are some illustration of impedance controlled RF trace designing. It is should be noted that the RF trace's width and spacing to the reference ground is combined to specific PCB stack-up(the PCB's thickness, clearance between every layer).

6.2.1 Two-layers PCB

The board thinkness is 0.8mm.



number	Details for calculation	Total thick-ess averag	After press nominal
	soldermask		10(min)
1	Copper	12+plating	25~48
1	PP	700	700
1	Copper	12+plating	25~48
	soldermask		10(min)
TOTAL			800

unit:um

finish thickness =0.8mm

SIG layer	GND layer	Target Imp.	Expected Width
L1	L2	50 Ω	1.35MM（53MIL）
L2	L1	50 Ω	1.35MM（53MIL）

The board thinkness is 1.0mm.

number	Details for calculation	Total thick-ess averag	After press nominal
	soldermask		10(min)
1	Copper	12+plating	25~48
1	PP	900	900
1	Copper	12+plating	25~48
	soldermask		10(min)
TOTAL			1000

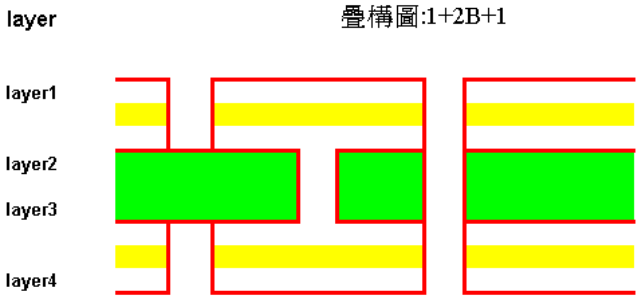
unit:um

finish thickness =1.0mm

SIG layer	GND layer	Target Imp.	Expected Width
L1	L2	50 Ω	1.7MM（67MIL）
L2	L1	50 Ω	1.7MM（67MIL）

6.2.2 Four-layers PCB

The board thinkness is 0.8mm.



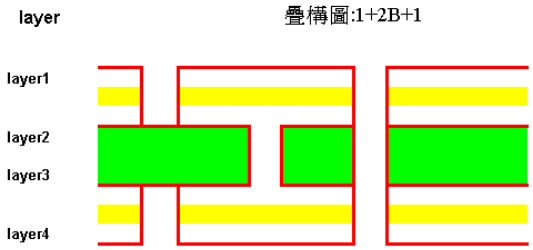
number	Details for calculation	Total thick-ess averag	After press nominal
	soldermask		10(min)
1	Copper	12+plating	25~48
1	PP	76	70
	copper	18+plating	25~48
1	core0.465r	465	465
	copper	18+plating	25~48
1	PP	76	70
1	Copper	12+plating	25~48
	soldermask		10(min)
TOTAL			800

unit:um

finish thickness =0.8mm

RF Signal layer	reference GND layer	Target Imp.	Expected RF Trace Width
L1	L2	50 Ω	0.114MM（4.5MIL）
L4	L3	50 Ω	0.114MM（4.5MIL）
L2	L1，L3	50 Ω	0.099MM（3.9MIL）
L3	L2，L4	50 Ω	0.099MM（3.9MIL）

The board thinkness is 1.0mm.



number	Details for calculation	Total thick-ess averag	After press nominal
	soldermask		10(min)
1	Copper	12+plating	25~48
1	PP	76	70
	copper	18+plating	25~48
1	core0.665r	665	665
	copper	18+plating	25~48
1	PP	76	70
1	Copper	12+plating	25~48
	soldermask		10(min)
TOTAL			1000

unit:um

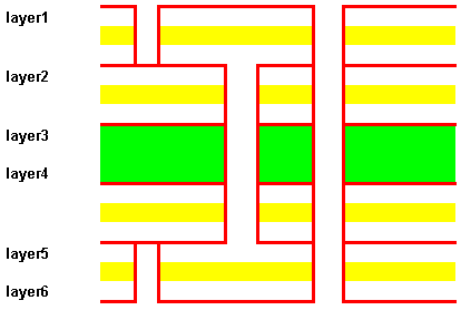
finish thickness =1.0mm

RF Signal layer	reference GND layer	Target Imp.	Expected RF Trace Width
L1	L2	50 Ω	0.114MM（4.5MIL）
L4	L3	50 Ω	0.114MM（4.5MIL）
L2	L1，L3	50 Ω	0.099MM（3.9MIL）
L3	L2，L4	50 Ω	0.099MM（3.9MIL）

6.2.3 Six-layers PCB

The board thinkness is 1.0mm.

layer 疊構圖:1+4B+1



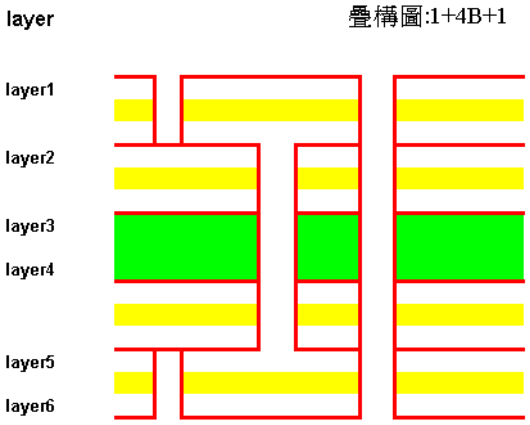
	soldermask		10(min)
1	Copper	12+plating	25~48
1	PP	76	70
1	copper	18+plating	25~48
1	PP	208	203
			35
1	core0.18m	180	180
			35
1	PP	208	203
1	copper	18+plating	25~48
1	PP	76	70
1	Copper	12+plating	25~48
	soldermask		10(min)
TOTAL			1000

unit:um

finish thickness =1.0mm

SIG layer	GND layer	Target Imp.	Expected Width
L1	L2	50 Ω	0.114MM（4.5MIL）
L1	L3	50 Ω	0.584MM（23MIL）
L6	L5	50 Ω	0.114MM（4.5MIL）
L6	L4	50 Ω	0.584MM（23MIL）
L3	L2，L4	50 Ω	0.135MM（5.3MIL）
L3	L2，L5	50 Ω	0.210MM（8.3MIL）
L4	L3，L5	50 Ω	0.135MM（5.3MIL）
L4	L2，L5	50 Ω	0.210MM（8.3MIL）

The board thinkness is 1.2mm.



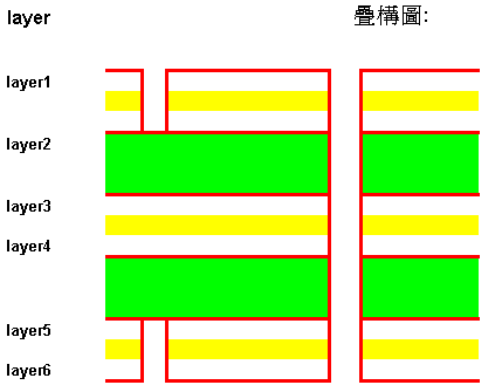
number	Details for calculation	Total thick-ess averag	After press nominal
	soldermask		10(min)
1	Copper	12+plating	25~48
1	PP	76	70
1	copper	18+plating	25~48
1	PP	132	127
			17
1	core0.565r	565	565
			17
1	PP	132	127
1	copper	18+plating	25~48
1	PP	76	70
1	Copper	12+plating	25~48
	soldermask		10(min)
TOTAL			1200

unit:um

finish thickness =1.2mm

RF Signal layer	Reference GND layer	Target Impedance	Expected RF Trace Width
L1	L2	50 Ω	0.114MM（4.5MIL）
L1	L3	50 Ω	0.42MM（16.5MIL）
L6	L5	50 Ω	0.114MM（4.5MIL）
L6	L4	50 Ω	0.42MM（16.5MIL）
L3	L2，L4	100 Ω	0.305MM（12.5MIL）
L3	L2，L5	100 Ω	0.381MM（15MIL）
L4	L3，L5	100 Ω	0.305MM（12.5MIL）
L4	L2，L5	100 Ω	0.381MM（15MIL）

The board thinkness is 1.6mm.



number	Details for calculation	Total thick-ess averag	After press nominal
	soldermask		10(min)
1	Copper	12+plating	25~48
1	PP	76	70
1		18	17
1	core0.51m	510	510
		18	17
			17
1	PP	231	220
		18	17
1	core0.51m	510	510
1		18	17
1	PP	76	70
1	Copper	12+plating	25~48
	soldermask		10(min)
TOTAL			1600

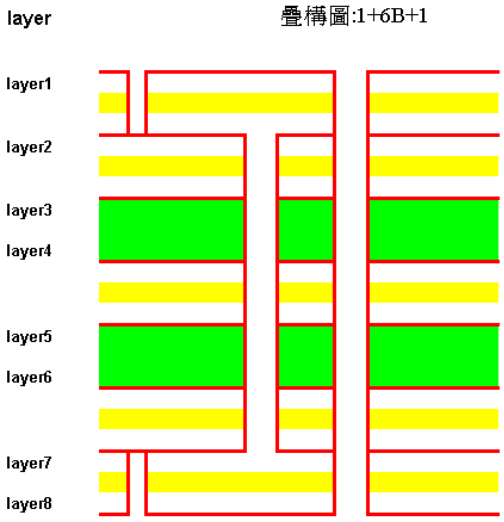
unit:um

finish thickness =1.6mm

RF Signal layer	Reference GND layer	Target Impedance	Expected RF Trace Width
L1	L2	50 Ω	0.114MM（4.5MIL）
L6	L5	50 Ω	0.114MM（4.5MIL）
L3	L2，L4	50 Ω	0.305MM（12MIL）
L3	L2，L5	75 Ω	0.246MM（9.7MIL）
L4	L3，L5	50 Ω	0.305MM（12MIL）
L4	L2，L5	75 Ω	0.246MM（9.7MIL）

6.2.4 Eight-layers PCB

The board thinkness is 1.0mm.



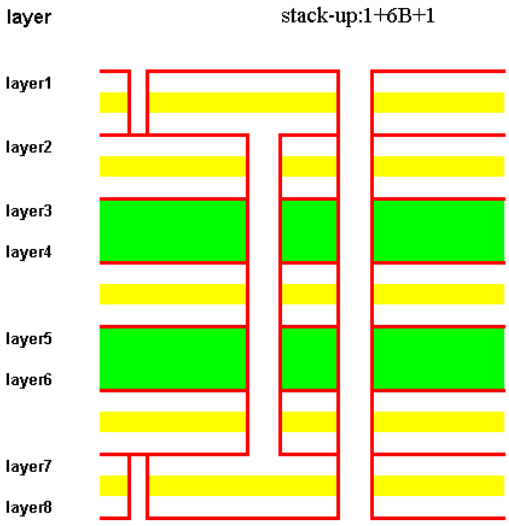
number	Details for calculation	Total thick-ness average	After press nominal
	soldermask		10(min)
1	Copper	12+plating	25~48
1	PP	76	70
1	copper	18+plating	25~48
1	PP	76	70
			17
1	core0.18mmH/H	180	180
			17
1	PP	76	70
			17
1	core0.18mmH/H	180	180
			17
1	PP	76	70
1	copper	18+plating	25~48
1	PP	76	70
1	Copper	12+plating	25~48
	soldermask		10(min)
TOTAL			1000

unit:um

finish thickness =1.0mm

RF Signal layer	Reference GND layer	Target Impedance	Expected RF Trace Width
L1	L2	50 Ω	0.114MM（4.5MIL）
L1	L3	50 Ω	0.3MM（11.8MIL）
L8	L7	50 Ω	0.114MM（4.5MIL）
L8	L6	50 Ω	0.3MM（11.8MIL）
L3	L2，L4	50 Ω	0.0965（3.8MIL）
L3	L2，L5	50 Ω	0.104MM（4.1MIL）
L4	L3，L5	50 Ω	0.0965（3.8MIL）
L4	L2，L5	50 Ω	0.104MM（4.1MIL）
L4	L2，L7	50 Ω	0.305MM（12MIL）
L6	L5，L7	50 Ω	0.0965（3.8MIL）
L6	L4，L7	50 Ω	0.104MM（4.1MIL）
L5	L4，L6	50 Ω	0.0965（3.8MIL）
L5	L4，L7	50 Ω	0.104MM（4.1MIL）

The board thinkness is 1.2mm.



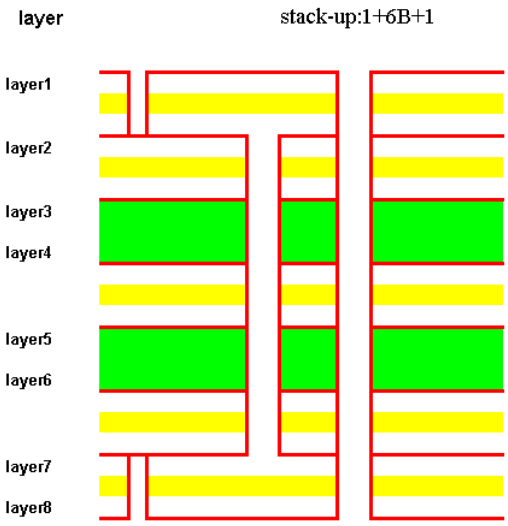
	Details for calculation	Total thick-ness average	After press nominal
	soldermask		10(min)
layer1	Copper	12+plating	25~48
dielectric	PP	76	70
layer2	copper	18+plating	25~48
dielectric	PP	119	114
layer3			17
dielectric	core0.18mmH/H	180	180
layer4			17
dielectric	PP	210	203
layer5			17
dielectric	core0.18mmH/H	180	180
layer6			17
dielectric	PP	119	114
layer7	copper	18+plating	25~48
dielectric	PP	76	70
layer8	Copper	12+plating	25~48
	soldermask		10(min)
TOTAL			1200

unit:um

finish thickness =1.2mm

RF Signal layer	Reference GND layer	Target Impedance	Expected RF Trace Width
L1	L2	50 Ω	0.114MM（4.5MIL）
L1	L3	50 Ω	0.394MM（15.5MIL）
L8	L7	50 Ω	0.114MM（4.5MIL）
L8	L6	50 Ω	0.394MM（15.5MIL）
L3	L2，L4	50 Ω	0.135（5.3MIL）
L3	L2，L5	50 Ω	0.165MM（6.5MIL）
L4	L3，L5	50 Ω	0.185（7.3MIL）
L4	L2，L5	50 Ω	0.24MM（9.5MIL）
L6	L5，L7	50 Ω	0.135（5.3MIL）
L6	L4，L7	50 Ω	0.165MM（6.5MIL）
L5	L4，L6	50 Ω	0.185（7.3MIL）
L5	L4，L7	50 Ω	0.24MM（9.5MIL）

The board thinkness is 1.6mm.



number	Details for calculation	Total thick-ness average	After press nominal
	soldermask		10(min)
layer1	Copper	12+plating	25~48
dielectric	PP	76	70
layer2		18+plating	25~48
dielectric	core0.365mm H/H	365	365
layer3		18	17
dielectric	PP	76	70
layer4		18	17
dielectric	core0.365mm H/H	365	365
layer5		18	17
dielectric	PP	76	70
layer6		18	17
dielectric	core0.365mm H/H	365	365
layer7		18+plating	25~48
dielectric	PP	76	70
layer8	Copper	12+plating	25~48
	soldermask		10(min)
TOTAL			1600

unit:um

finish thickness =1.6mm

RF Signal layer	Reference GND layer	Target Impedance	Expected RF Trace Width
L1	L2	50 Ω	0.114MM（4.5MIL）
L8	L7	50 Ω	0.114MM（4.5MIL）
L3	L2，L4	50 Ω	0.11（4.3MIL）
L3	L2，L5	50 Ω	0.432MM（17MIL）
L4	L3，L5	50 Ω	0.11（4.3MIL）
L4	L2，L5	50 Ω	0.432MM（17MIL）
L6	L5，L7	50 Ω	0.11（4.3MIL）
L6	L4，L7	50 Ω	0.432MM（17MIL）
L5	L4，L6	50 Ω	0.11（4.3MIL）
L5	L4，L7	50 Ω	0.432MM（17MIL）

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